We claim:

1. A differential transistor pair, comprising a plurality of transistor cells in a substrate, each cell comprising:

- first drain/collector regions at the respective edge of the cell,

- a second drain/collector region between the first drain/collector regions,

- source/emitter regions between the respective first drain/collector region and the second drain/collector region,

- first gate/base regions between the respective first drain/collector region and the source/emitter regions, and

- second gate/base regions between the source/emitter regions and the second drain/collector region, wherein

the first drain/collector regions of all cells being interconnected to a common first drain/collector terminal,

the second drain/collector region of all cells being interconnected to a common second drain/collector terminal,

the first gate/base regions of all cells being interconnected to a common first gate/base terminal, and

the second gate/base regions of all cells being interconnected to a common second gate/base terminal.

2. A transistor cell in a substrate comprising:

- first drain/collector regions at the respective edge of the cell,

- a second drain/collector region between the first drain/collector regions,

- source/emitter regions between the respective first drain/collector region and the second drain/collector region,

- first gate/base regions between the respective first drain/collector region and the source/emitter regions, and

- second gate/base regions between the source/emitter regions and the second drain/collector region, wherein

the first drain/collector regions of all cells being interconnected to a common first drain/collector terminal,

the second drain/collector region of all cells being interconnected to a common second drain/collector terminal,

the first gate/base regions of all cells being interconnected to a common first gate/base terminal, and

the second gate/base regions of all cells being interconnected to a common second gate/base terminal.

3. A bipolar differential transistor pair, comprising a plurality of transistor cells in a substrate, each cell comprising:

- first collector regions at the respective edge of the cell,

- a second collector region between the first collector regions,

- emitter regions between the respective first collector region and the second collector region,

- first base regions between the respective first collector region and the emitter regions, and

- second base regions between the emitter regions and the second collector region, wherein

the first collector regions of all cells being interconnected to a common first collector terminal,

the second collector region of all cells being interconnected to a common second collector terminal,

the first base regions of all cells being interconnected to a common first base terminal, and

the second base regions of all cells being interconnected to a common second base terminal.